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-	1	US20030145255A1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2004/10/27 11:34
-	2	5274811.pn.	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2004/10/27 11:38
-	2	5446876.pn.	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2004/10/27 11:41
-	2	5642478.pn.	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2004/10/27 11:42
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-	2	6055492.pn.	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 12:07

	94	( "6021457" "5642478" "5471526" "5594904" "5996092" "6173395" "6349406" "6662358" "5386565" "6055492" "6205492" "4590550" "5297274" "5862381" "5680583" "5884066" "6493837" "6002872" "6158024" "4821178" "5430875" "5386582" "5970246" "5218707" "6226787" "6226787" "6397379" "6549959" "6779107" "6789181" "5621886" "5740413" "6016558" "6332117" "5280593" "5822585" "6240529" "6338159" "6807583" "5802272" "3707725" "5946486" "5944841" "6253338" "6738965" "4924466" "5450586" "5513338" "5845106" "6209041").pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 12:12
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	1	buffer\$1 with per with type\$1 with event\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:16
	0	6633961.URPN.	USPAT	2004/10/27 16:18
	3	("5333269"   "5619500"   "5664116").PN.	USPAT	2004/10/27 16:19
	414	717/124.cc1s.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/10/29 10:10

-	325	717/127.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT	2004/10/29 10:10
-	276	717/128.ccls.		2004/10/29 10:10
-	2	("4811278"   "5613082").PN.		2004/10/29 10:10
-	0	6405329.URPN.	USPAT	2004/10/29 10:12



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Relevance scale

- 1** [Memory consistency and event ordering in scalable shared-memory multiprocessors](#)

Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, John Hennessy

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture**, Volume 18 Issue 3

Full text available: [pdf\(1.56 MB\)](#)

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Scalable shared-memory multiprocessors distribute memory among the processors and use scalable interconnection networks to provide high bandwidth and low latency communication. In addition, memory accesses are cached, buffered, and pipelined to bridge the gap between the slow shared memory and the fast processors. Unless carefully controlled, such architectural optimizations can cause memory accesses to be executed in an order different from what the programmer expects. The set of allowable ...

- 2** [Memory consistency and event ordering in scalable shared-memory multiprocessors](#)

Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, John Hennessy

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: [pdf\(1.66 MB\)](#)

Additional Information: [full citation](#), [references](#), [index terms](#)

- 3** [Fast detection of communication patterns in distributed executions](#)

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: [pdf\(4.21 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

- 4** [A structural view of the Cedar programming environment](#)

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann

August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**,

Volume 8 Issue 4